In The Claims:

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A method of correcting a clock of a compact disk, comprising:

receiving a data signal and a clock signal;

generating a sync pattern signal by using the clock signal to detect the data signal;

generating a detection window signal according to a clock number during a timing of a last sync pattern signal and a first preset timing, the detection window signal having a second preset timing width; and

comparing a clock of the sync pattern signal with the detection window signal, and correcting the clock signal;

wherein one end of the detection window signal adjacent to a last detection window signal is a signal front-edge, another end of the detection window signal is a signal post-edge, a region of the detection window signal within a third preset timing adjacent to the signal front-edge is a front-edge region, a region of the detection window signal within a fourth preset timing adjacent to the signal post-edge is a post-edge region, a sum of the third preset timing and the fourth preset timing is no more than the second preset timing, the step of comparing the clock of the sync pattern signal with the detection window signal further comprising:

determining whether the sync pattern signal is in the front-edge region, wherein if it is, a

frequency-increase signal is sent out;

determining whether the sync pattern signal is in the post-edge region, wherein if it is, a frequency-reduction signal is sent out;

determining whether the sync pattern signal is between the front-edge region and the post-edge region, wherein if it is, a frequency-remain signal is sent out; and

correcting the clock signal according to the frequency-increase signal, the frequency-reduction signal and the frequency-remain signal.

2. (original) The method of correcting a clock of a compact disk of claim 1, wherein the sync pattern signal is generated when the clock signal and the data signal change from zero to non-zero simultaneously.

3. (original) The method of correcting a clock of a compact disk of claim 1, wherein the sync pattern signal is generated when the clock signal and the data signal change from non-zero to zero simultaneously.

Claim 4. (canceled)

5. (currently amended) The method of correcting a clock of a compact disk of claim [[4]] 1, further comprising a fifth preset timing with a frequency-lock region between the front-edge region and the post-edge region, a sum of the third preset timing, the fourth timing and the fifth

timing is no more than the second preset timing.

6. (original) The method of correcting a clock of a compact disk of claim 5, further comprising determining whether the sync pattern signal is in the frequency-lock region, wherein if it is, the frequency-remain signal is sent out.

7. (original) The method of correcting a clock of a compact disk of claim 6, wherein the step of correcting the clock signal according to frequency-increase signal, the frequency-reduction signal and the frequency-remain signal further comprising:

measuring and determining whether a number of the frequency-increase signal is larger than a first preset counting number, wherein if it is, a frequency–increase trigger signal is generated and the number of the frequency-increase signal is reset;

measuring and determining whether a number of the frequency-reduction signal is larger than a second preset counting number, wherein if it is, a frequency–reduction trigger signal is generated and the number of the frequency-reduction signal is reset;

measuring and determining whether a number of the frequency-remain signal is larger than a third preset counting number, wherein if it is, a frequency–remain trigger signal is generated and the number of the frequency-remain signal is reset; and

correcting the clock signal according to the frequency-increase trigger signal, the frequency-reduction trigger signal and the frequency-remain trigger signal.

8. (original) The method of correcting a clock of a compact disk of claim 7, wherein the first preset counting number, the second preset counting number and the third preset counting number are the same preset counting number.

9. (original) The method of correcting a clock of a compact disk of claim 7, wherein the first preset counting number, the second preset counting number and the third preset counting number are different from each other.

10. (currently amended) A circuit for correcting a clock of a compact disk, comprising:

a synchronous detecting circuit, adapted to receive a clock signal and a data signal for generating a sync pattern signal by using the clock signal to detect the data signal;

a detection window generator, adapted to receive the clock signal and the sync pattern signal for generating a detection window signal according to a clock number during a timing of a last sync pattern signal and a first preset timing, the detection window signal having a second preset timing width; and

a synchronous phase detecting circuit, adapted to receive the sync pattern signal and the detection window signal for comparing a clock of the sync pattern signal with the detection window signal, and generating a frequency-correcting signal according to the compare result for correcting the clock signal~~.~~

wherein one end of the detection window signal adjacent to a last detection window signal is a signal front-edge, another end of the detection window signal is a signal post-edge, a

region of the detection window signal within a third preset timing adjacent to the signal front-edge is a front-edge region, a region of the detection window signal within a fourth preset timing adjacent to the signal post-edge is a post-edge region, a sum of the third preset timing and the fourth preset timing is no more than the second preset timing, the synchronous phase detecting circuit comprising:

a timing-position detector, adapted to receive and determine whether a relationship between the sync pattern signal and the detection window signal, sending out a frequency-increase signal, a frequency-reduction signal or a frequency-remain signal according to a location of the sync pattern signal in the front-edge region, the post-edge region, or between the front-edge region and the post-edge region, respectively; and

a frequency-correcting module, adapted to receive the frequency-increase signal, the frequency-reduction signal and the frequency-remain signal, and generate the frequency-correcting signal.

11. (original) The circuit for correcting a clock of a compact disk of claim 10, wherein the sync pattern signal is generated when the clock signal and the data signal change from zero to non-zero simultaneously.

12. (original) The circuit for correcting a clock of a compact disk of claim 10, wherein the sync pattern signal is generated when the clock signal and the data signal change from non-zero to zero simultaneously.

Claim 13. (canceled)

14. (currently amended) The circuit for correcting a clock of a compact disk of claim [[13]] 10, wherein the frequency-correcting module comprises:

an ahead counter, adapted to receive the frequency-increase signal, measure a number of the frequency-increase signal, send out an ahead counting number, and reset the number of the frequency-increase signal while receiving a first reset signal;

a moderate counter, adapted to receive the frequency-remain signal, measure a number of the frequency-remain signal, send out a moderate counting number, and reset the number of the frequency-remain signal while receiving a second reset signal;

a behind counter, adapted to receive the frequency-reduction signal, measure a number of the frequency-reduction signal, send out a behind counting number, and reset the number of the frequency-reduction signal while receiving a third reset signal;

a frequency-increase trigger, adapted to receive and check the ahead counting number, moreover, adapted to generate the first reset signal and a frequency-increase trigger signal if the ahead counting number is larger than a first preset number;

a frequency-remain trigger, adapted to receive and check the moderate counting number, moreover, adapted to generate the second reset signal and a frequency-remain trigger signal if the moderate counting number is larger than a second preset number;

a frequency-reduction trigger, adapted to receive and check the behind counting number, moreover, adapter to generate the third reset signal and a frequency-reduction trigger signal if the

behind counting number is larger than a third preset number; and

a frequency corrector, adapted to receive the frequency-increase trigger signal, the frequency-reduction trigger signal and the frequency-remain trigger signal, and generate the frequency-correcting signal.

15. (original) The circuit for correcting a clock of a compact disk of claim 14, wherein the first preset counting number, the second preset counting number and the third preset counting number are the same preset counting number.

16. (original) The circuit for correcting a clock of a compact disk of claim 14, wherein the first preset counting number, the second preset counting number and the third preset counting number is different to each other.